Electrical Properties and Stability of Dual-Gate Coplanar Homojunction DC Sputtered Amorphous Indium–Gallium–Zinc–Oxide Thin-Film Transistors and Its Application to AM-OLEDs

Gwanghyeon Baek, Katsumi Abe, Alex Kuo, Hideya Kumomi, and Jerzy Kanicki

***Abstract*—The electrical characteristics and stability of dual–gate (DG) coplanar homojunction amorphous indium–gallium–zinc–oxide thin-film transistors (a-IGZO TFTs) on glass substrates are described herein. In this device structure, both top gate (TG) and bottom gate are defined by lithography, allowing independent biasing when adjacent TFTs are present. The DG a-IGZO TFT demonstrates excellent electrical performance with subthreshold swing (SS) of 99 mV/dec, field-effect mobility of 15.1 $\mathrm{cm^2/V \cdot s}$, and ON–OFF current ratio of 10^9. By applying various bias voltages on the TG electrode, it is found that the TFT threshold voltage can be controlled without any change of the SS and off current. Under conditions of negative bias temperature stress (BTS), the transfer curves of the TFT exhibit negligible shifts after 10 000 s. Larger shifts are observed under conditions of a positive BTS. Finally, the application of this DG device to active-matrix organic light-emitting displays is suggested.**

***Index Terms*—Active-matrix organic light-emitting display (AM-OLED), amorphous indium–gallium–zinc–oxide (a-IGZO), coplanar homojuction, dual gate (DG), thin-film transistor (TFT).**

I. Introduction

AMORPHOUS indium-gallium-zinc-oxide thin-film transistors (a-IGZO TFTs) have been considered as a very serious candidate for high-resolution large-area active-matrix flat-panel displays (AM-FPDs) [1], [2]. This is due to their high field-effect mobility μ_{EFF}, low leakage current I_{OFF}, good electrical stability, superior optoelectronic characteristics, and low temperature fabrication [3]–[5].

It is well known that the electrical performance of metal–oxide–semiconductor field-effect transistors (MOSFETs) is improved when a larger portion of the channel area is controlled by an additional gate electrode [6]. Dual-gate (DG) amorphous silicon (a-Si:H) TFTs have also been proposed to provide effective light shielding to prevent the degradation of the TFT's electrical properties under illumination [7], [8]. However, the presence of bias on the additional gate electrode introduces unwanted increases in the a-Si:H TFT's subthreshold swing (SS) and off current I_{OFF}. To address this problem, the additional gate electrode has been grounded to provide stable circuit operation in a pixel array [9], [10].

Several results on DG a-IGZO TFTs have recently been reported [11]–[15]. The device structures described in [11]–[14] have defined the top gate (TG) but have left the bottom gate (BG) undefined, i.e., a common BG is used in all the reported TFTs. This type of device structure is simple to fabricate and somewhat useful for fundamental property investigation. Since the undefined BG (very often made of heavily doped silicon wafers) in such a device covers the whole substrate area, it is impossible to apply a different gate bias voltage on adjacent TFTs when large numbers of TFTs are fabricated on the same substrate. To investigate the usefulness of DG a-IGZO TFT application to AM-FPD, a device structure with well-defined gates is required. This will allow us to apply independent gate bias voltage on both TG and BG during the device property investigation and/or pixel circuit operation. In [15], Son *et al.* described the DG a-IGZO TFT with defined TG and BG electrodes. In their structure, amorphous silicon nitride $(\mathrm{a\text{-}SiN}_x)$ is used for the BG insulator, and amorphous silicon oxide $(\mathrm{a\text{-}SiO}_x)$ is used for the TG insulator. To take advantage of the DG structure, it is important to optimize the nature of the dielectrics and gate insulator–semiconductor interfaces used in such a device. Son *et al.* tried only to extend the gate dielectric technology developed for a-Si:H TFTs to a-IGZO TFTs without providing any proper device physics-based justifications.

It was previously reported that the coplanar homojunction a-IGZO TFT has good ohmic source/drain (S/D) junction and is capable of achieving small (5 μm or less) channel lengths. [16], [17]. In this paper, we describe the electrical characteristics and stability of DG coplanar homojunction a-IGZO TFT. In this structure, the TG and BG electrodes are defined, enabling independent electrode biasing. The $\mathrm{a\text{-}SiO}_x$ is used for both TG and BG insulators, since it was shown in the past that a-IGZO TFTs with $\mathrm{a\text{-}SiO}_x$ gate dielectric exhibit better electrical performance and stability than the TFT with $\mathrm{a\text{-}SiN}_x$ [18]. Herein we describe the device electrical properties in the dark

Manuscript received December 16, 2010; revised March 10, 2011, May 2, 2011, May 31, 2011, July 7, 2011, July 20, 2011, and August 23, 2011; accepted August 24, 2011. Date of current version November 23, 2011. This work was supported in part by Cannon Research Center, Japan, and in part by Applied Materials, USA. The review of this paper was arranged by Editor H.-S. Tae.

G. Baek, A. Kuo, and J. Kanicki are with the Displays and Detectors Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA (e-mail: kanicki@eecs.umich.edu).

K. Abe and H. Kumomi are with the Canon Research Center, Canon Inc., Tokyo 146-8501, Japan.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2011.2168528

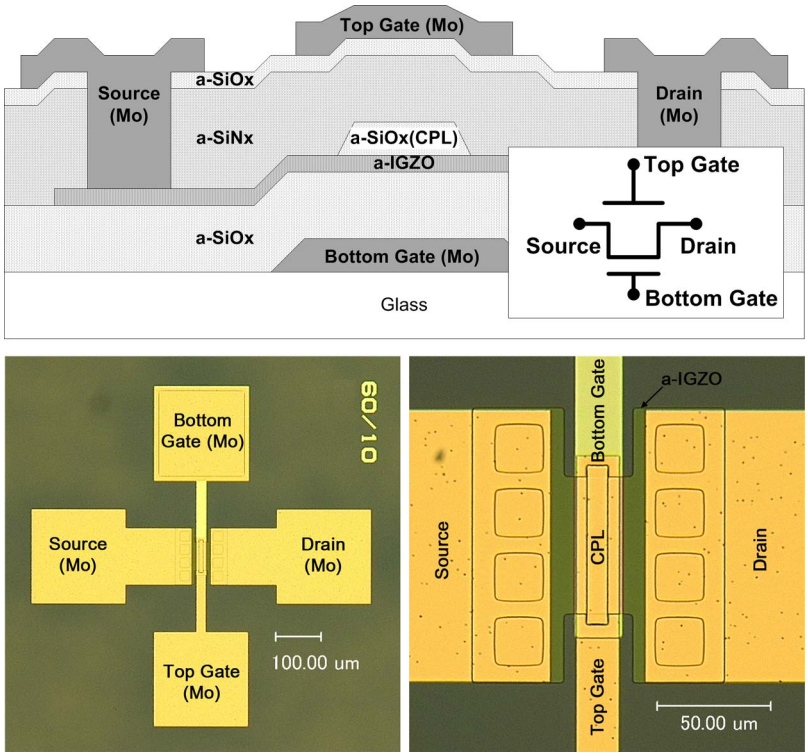

Fig. 1. (Top) Cross-section of DG a-IGZO TFT used in this paper. (Bottom) Microscopic image of the fabricated device.

and under illumination. We discuss the device threshold voltage controllability through TG voltage application. This method is referred to as dynamic control of the DG TFT threshold voltage. We also report on the electrical stability of DG a-IGZO TFTs through bias temperature stress (BTS) studies. Finally, we discuss the application of this device to active-matrix organic light-emitting displays (AM-OLEDs) as new pixel electrode circuits with expected superior electrical performance and stability in comparison with a-Si:H TFT pixel circuits.

II. Experimental

Fig. 1 shows the schematic cross-section and microscopic top view of the DG coplanar homojunction a-IGZO TFT used in this paper. The TFT's BG electrode was fabricated from sputtered molybdenum (100 nm) on a glass substrate. Plasma-enhanced chemical vapor deposition (PECVD) was used to deposit the a-SiO_x gate insulator (200 nm). The a-IGZO film (30 nm) was dc sputtered and defined using wet etching with diluted hydrochloric acid. A 150-nm sputtered a-SiO_x (has negligible hydrogen content) channel protection layer (CPL) was rf sputtered and patterned by photolithography and dry etching. The CPL defines the TFT width W and length L: $W = 60\ \mu$m and $L = 10\ \mu$m. The CPL patterning was followed by a PECVD passivation of 300-nm-thick a-SiN_x : H and 50-nm-thick a-SiO_x at the substrate temperature of 250 °C. During the a-SiN_x : H PECVD process, hydrogen present in the PECVD reactive chamber and/or in the hydrogen-rich a-SiN_x : H layer dopes the exposed a-IGZO region and increases its electrical conductivity [16], [17]. Effectively heavily hydrogen-doped a-IGZO regions outside of the CPL are formed, to be used as source/drain (S/D) contact regions. Next, S/D contact vias were formed in the top passivation layer by dry etching, followed by the sputtering and patterning of 100-nm-thick Mo source/drain electrodes. At the same time, the Mo TG is formed. It should be noticed that in such device structure, Mo metal gate and source/drain contacts do not overlap, although there is some overlap between Mo metal gate and the hydrogen doped S/D contact regions. There is separation of about 20 μm between CPL edge and S/D via edge. All lithographic patterning use S-1813 positive tone photoresist. Finally, the TFT underwent a thermal annealing step at 270 °C in atmosphere at the end of the device process.

All the TFTs' electrical transfer characteristics were measured using an Agilent 4156C with the source acting as the ground and a gate-to-source voltage $V_{\rm GS}$ sweeping from -10 to 15 and from 15 to -10 V at 0.2 V intervals. The reverse direction sweeping of $V_{\rm GS}$ is used to check for device hysteresis. For the dynamic control of a threshold voltage $V_{\rm TH}$, we applied $V_{\rm GS}$ on a TG electrode ranging from -4 to 4 V at 2 V intervals during the transfer characteristic measurements.

During the BTS experiment, the stress voltages $V_{\rm STR} = +15$ or -15 V are used for positive BTS (PBTS) and negative BTS (NBTS), respectively, and the drain and source terminals are shorted together during BTS. For DG TFT stress, the stress voltage is applied on the TG and BG at the same time, i.e., $V_{\rm STR} = V_{\rm BG} = V_{\rm TG}$. During single-gate TFT BTS, the stress voltage is applied on one gate, and another gate is grounded. The stress temperature is fixed at 80 °C. All the BTS-induced electrical instabilities can fully be recovered after a thermal annealing step. Each series of BTS experiment is performed on the same TFT to ensure consistent initial (before BTS) TFT properties, and the thermal annealing step is applied before each new BTS experiment is conducted.

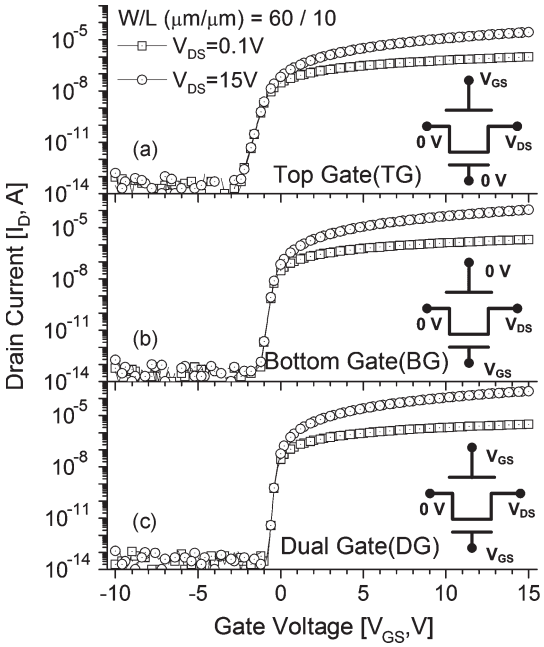

Fig. 2. Transfer characteristics of DG coplanar homojunction a-IGZO TFTs for three different bias conditions. (a) TG. (b) BG. (c) DG biasing.

Finally, we expose the top surface of TFTs (with and without gate electrode present) to Mercury-Xeon (Oriel 6291) arc lamp through a microscope via a fiber optic (with 10 mW/cm^2 of illumination) [19]. The wavelength λ of the illuminated light has the spectral range from 200 to 2400 nm.

III. Experimental Results and Discussion

Figs. 2 and 3 show the transfer and output characteristics of DG a-IGZO TFT with three different gate bias conditions. Fig. 2(a) and (b) is measured by applying gate voltage only on TG or BG, respectively, whereas the other gate is grounded. In Fig. 2(c), identical gate voltage is applied and swept on both TG and BG electrodes at the same time. We call this device configuration: synchronized bias or DG bias condition. In all three gate bias conditions, TFT demonstrates normal TFT operation. Fig. 3(b) shows details of the output curves for a small drain-to-source voltage $V_{\rm DS}$ region, 0 V $\leq V_{\rm DS} \leq$ 1 V; no current crowding is found near the origin. Hence, it can be concluded from these data that the Mo/a-IGZO source/drain contact is ohmic in nature [20]. The electron affinities of Mo and undoped a-IGZO are 4.3–4.7 and 4.16–4.3 eV, respectively [21], [22]; hence, the expected Schottky barrier height for such contact is less than 0.4 eV.

To extract device parameters, such as field-effect mobility $\mu_{\rm EFF}$ and threshold voltage $V_{\rm TH}$, the standard MOSFET drain current equation is used in the linear regime of the device operation [23]

$$I_D = \mu_{\rm EFF} C_{\rm GI} \frac{W}{L} (V_{\rm GS} - V_{\rm TH}) V_{\rm DS} \quad (1)$$

where W and L are the channel width and length of the TFT, respectively. $C_{\rm GI}$ is the gate capacitance per unit area. Since the measured transfer curves have a very linear behavior,

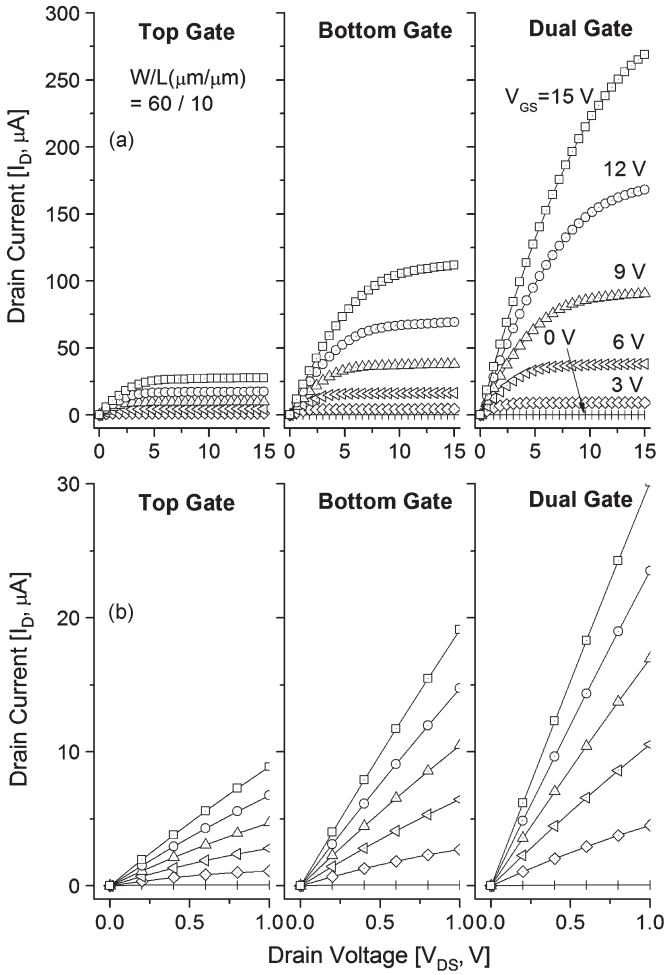

Fig. 3. Output characteristics of DG coplanar homojunction a-IGZO TFTs (a) for different bias conditions and (b) details shown for the 0 V $\leq V_{\rm DS} \leq$ 1 V.

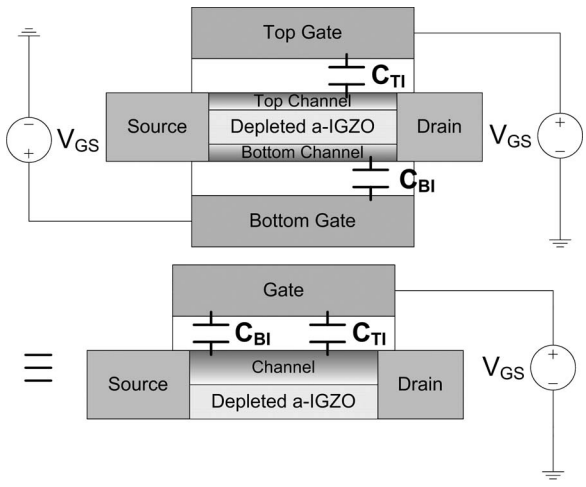

Fig. 4. Gate capacitance diagram for the DG configuration and its equivalent diagram.

the linear fitting method based on 10%–90% of maximum I_D is used. An example of the DG TFT parameter extraction is provided in [24].

The gate capacitances of TG $C_{\rm TI}$ and BG $C_{\rm BI}$ insulator can be calculated using the thickness $t_{\rm TI}$ or $t_{\rm BI}$ and dielectric

TABLE I
EXTRACTED DEVICE PARAMETERS FOR DG COPLANAR HOMOJUNCTION a-IGZO TFTs

	TG Bias		BG Bias		DG Bias	
	Lin.	Sat.	Lin.	Sat.	Lin.	Sat.
I_{ON} (V_{GS}=10V)	6.3×10^{-7}	1.2×10^{-5}	1.3×10^{-6}	4.7×10^{-5}	2.0×10^{-6}	1.1×10^{-4}
I_{OFF} [A]	$< 10^{-13}$		$< 10^{-13}$		$< 10^{-13}$	
V_{TH} [V]	0.42	– 0.31	0.54	0.13	0.55	0.37
SS [mV]	286	293	153	153	100	99
μ_{EFF} [cm^2/V·s]	11.52	3.98	12.82	9.11	13.08	15.07
Hysteresis [V]	0		0		0	
C_{GI} [nF/cm^2]	C_{TI} = 9.5		C_{BI} = 17.7		C_{DI} = 27.2	
N_{SS} [$eV^{-1}cm^{-2}$]	6.0×10^{10}		5.4×10^{10}		5.8×10^{10}	

constant $\varepsilon_{\rm TI}$ or $\varepsilon_{\rm BI}$ of the TG and BG insulators, respectively, i.e.,

$$C_{\rm TI} = \varepsilon_{\rm TI}/t_{\rm TI} \quad \text{and} \quad C_{\rm BI} = \varepsilon_{\rm BI}/t_{\rm BI}. \tag{2}$$

The gate capacitance of DG $C_{\rm DI}$ cannot simply be defined. The gate voltages applied on the TG and BG electrodes form channels on the top and bottom sides of the a-IGZO thin film (Fig. 4). Since these channels are connected together at the source and drain electrodes, we consider the a-IGZO film as a single metal plate connecting TG and BG insulators in parallel. Hence, the effective gate capacitance of DG configuration is

$$C_{\rm DI} = C_{\rm TI} + C_{\rm BI}. \tag{3}$$

The values of $C_{\rm TI}$, $C_{\rm BI}$, and $C_{\rm DI}$ are given in Table I. The ε values for a-SiO_x and a-SiN_x are $4 \cdot \varepsilon_0$ and $7 \cdot \varepsilon_0$, respectively. The thickness of the bottom silicon oxide is 200 nm; the TG insulator has a trilayer structure: a-SiO_x/a-SiN_x/a-SiO_x. The thickness of the trilayer is 150/300/50 nm, respectively. The capacitance of the trilayer is calculated using three serially connected capacitors.

The subthreshold slope (SS) can be extracted from the linear portion of the transfer characteristics using following equation:

$$\text{SS} = \left(\frac{\partial \log I_D}{\partial V_{\rm GS}}\right)^{-1}. \tag{4}$$

The drain current range from one order below to one order above around a maximum $\partial \log I_D/\partial V_{\rm GS}$ point is used to calculate the SS. For conventional single-gate TFTs, the SS is approximately given by

$$SS \cong (k_B T/q) \cdot ln10 \left(1 + \frac{C_{\rm BSS} + C_{\rm TSS}}{C_{\rm GI}}\right) \tag{5}$$

where k_B is the Boltzmann constant, T is the temperature in Kelvin, and q is the electron charge. $C_{\rm BSS}$ is the capacitance of the bottom channel interface state per unit area and is defined by $C_{\rm BSS} = q \cdot N_{\rm BSS}$, where $N_{\rm BSS}$ is the density of bottom interface trap states. $C_{\rm TSS}$ and $N_{\rm TSS}$ are the symbols for the top channel interface. The average interface trap density can be calculated by assuming $N_{\rm SS} = N_{\rm TSS} = N_{\rm BSS}$. Using the SS value for TG and BG configurations (286 and 153 mV/dec), the calculated $N_{\rm SS}$ is about 6.0 and 5.4×10^{10} $\text{eV}^{-1}\text{cm}^{-2}$, respectively. Moreover, the SS for DG configuration can be written as follows because of $C_{\rm GI} = C_{\rm DI} = C_{\rm BI} + C_{\rm TI}$ [(3)] [25]:

$$SS \cong (k_B T/q) \cdot ln10 \left(1 + \frac{C_{\rm BSS} + C_{\rm TSS}}{C_{\rm BI} + C_{\rm TI}}\right). \tag{6}$$

From the measured value (SS = 100 mV/dec), (6) leads to $N_{\rm SS} = 5.8 \times 10^{10}$ $\text{eV}^{-1}\text{cm}^{-2}$ for DG configuration. We can conclude that a steeper SS for DG configuration is due to the increased gate capacitance.

For a more quantitative comparison, the extracted TFT parameters for BG, TG, and DG device configurations are tabulated in Table I. From these data, we can conclude that the DG a-IGZO TFT has the best electrical performance in terms of smaller SS and higher $I_{\rm ON}$. Since for the DG bias condition two channels (one on top and one bottom side of a-IGZO layer) are formed at the same time, steeper SS and higher $I_{\rm ON}$ through increase of effective channel thickness are expected [26]. $I_{\rm OFF}$ is independent of the gate bias conditions and is below 0.1 pA. This low $I_{\rm OFF}$ is due to a very low hole density present in the a-IGZO channel. We did not observe any p-channel behavior up to -20 V.

In Fig. 5, we show a comparison between the sum of ON current for the TG and BG bias conditions ($I_{\rm ON\_TG} + I_{\rm ON\_BG}$) and ON-current for the DG bias condition ($I_{\rm ON\_DG}$). In the linear region ($V_{\rm DS} = 0.1$), the sum of $I_{\rm ON\_TG}$ and $I_{\rm ON\_BG}$ is comparable to $I_{\rm ON\_DG}$. However, in the saturation region ($V_{\rm DS} = 15$ V), $I_{\rm ON\_DG}$ is about 85% higher than the sum of $I_{\rm ON\_TG}$ and $I_{\rm ON\_BG}$. In addition, Fig. 3(a) shows that insufficient channel saturation takes place for the DG bias condition in comparison with either TG or BG biasing condition. We speculated that, in the linear region, top and bottom channels are formed separately at the top and bottom interfaces, and two channels contribute to the increase of $I_{\rm ON}$. In the saturation region, the interactions between TG and BG voltages confine the channels more strongly. Consequently, DG TFT requires a higher $V_{\rm DS}$ to reach drain saturation, in comparison with TG or BG TFTs. Hence, the ON current keeps increasing proportionally to $V_{\rm DS}$ until saturation takes place. Therefore, the extended linear region causes an 85% increase in the ON current of DG TFT.

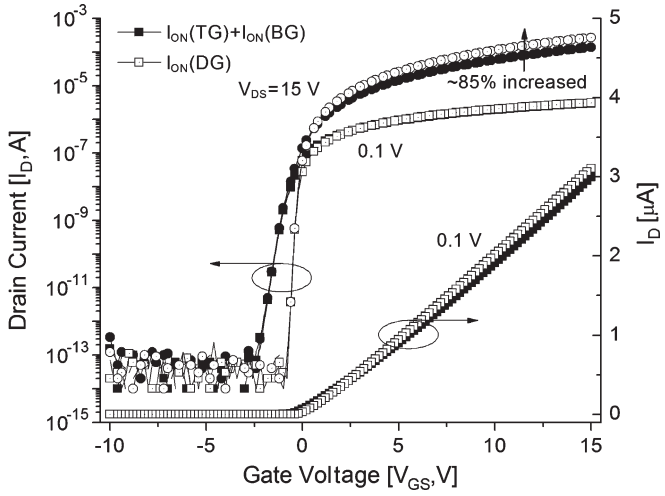

Fig. 5. Comparison between TFT on current for DG bias condition and the sum of TG and BG bias conditions.

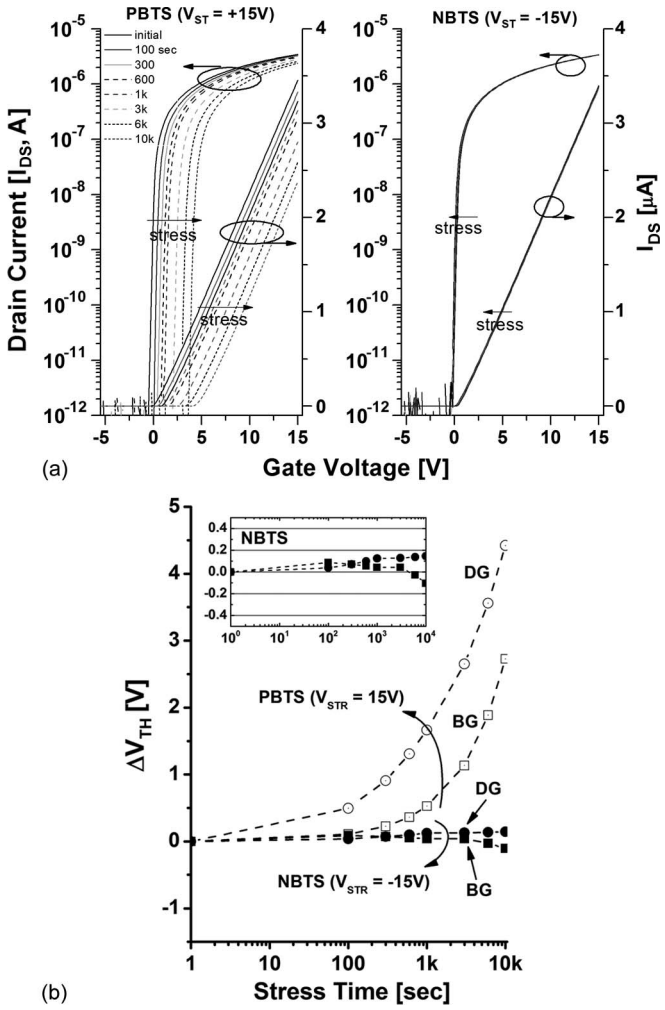

Fig. 6. (a) Variations of transfer curves of DG TFT during PBTS and NBTS at stress temperature of 80 °C. (b) Evaluation of $\Delta V_{\rm TH}$ with stress time for DG and BG conditions.

Fig. 6(a) shows the variations of transfer curves of DG a-IGZO TFT under PBTS and NBTS at 80 °C. When $+V_{\rm STR}$ is applied to TG and BG electrodes, $V_{\rm TH}$ is shifted from its original value to + 4.5 V. The shift of transfer curves under

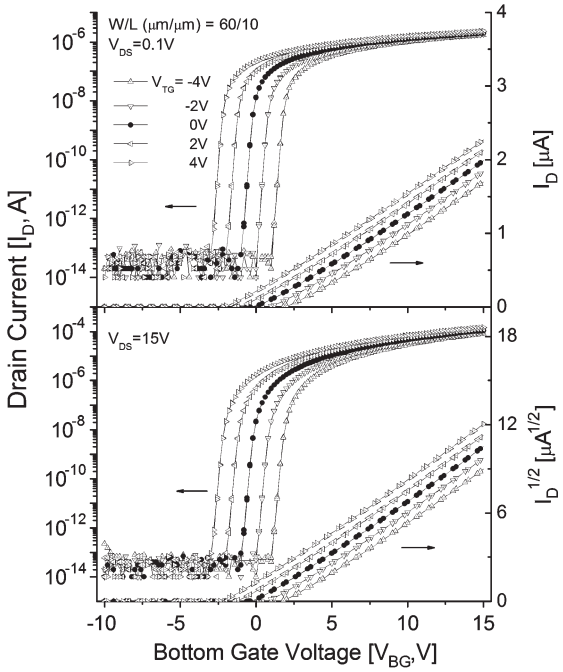

Fig. 7. Transfer characteristics of DG coplanar homojunction a-IGZO TFTs for various $V_{\rm TG}$ values.

NBTS is very small (smaller than 0.2 V). The evolution of $V_{\rm TH}$ shift ($\Delta V_{\rm TH}$) at 80 °C as a function of BTS time is summarized in Fig. 6(b). The observed $V_{\rm TH}$ shifts can be explained by the charge trapping mechanism. Under PBTS, the negative charges, e.g., electrons, are trapped at the top and bottom channel/insulator interfaces or into the gate insulator near these interfaces. In case of NBTS, the positive charges, e.g., holes, are trapped.

Since the numbers of holes in a-IGZO under NBTS condition is too small or the barrier energy for hole trapping is too large, it is expected for $\Delta V_{\rm TH}$ to be small. Moreover, Fig. 6(b) (inset) shows that, under NBTS, $V_{\rm TH}$ shifted first to the positive direction before shifting to the negative direction. This type of threshold voltage shift was also observed in a-Si TFT with a-SiO_x as gate insulator [27]. We also observed that under PBTS, the $\Delta V_{\rm TH}$ for DG TFTs is about two times larger than that for BG PBTS. Under different BTS conditions, such as bias condition or stress temperature, different, but consistent with each other, results are expected, as described in [25].

In the DG device structure, it is expected that the threshold voltage can be affected by the TG bias condition. Therefore, it is important to study the impact of the TG voltage $V_{\rm TG}$ on the DG a-IGZO TFT electrical properties. Fig. 7 shows the device transfer characteristics when a different $V_{\rm TG}$ is applied. We observed parallel shift of the transfer curves in response to $V_{\rm TG}$ without any changes of SS and $I_{\rm OFF}$. To explain this observation, it is worth to compare our results with those obtained for DG a-Si TFTs. In a-Si TFT, the magnitude of $V_{\rm TH}$ shift is smaller, and SS and $I_{\rm OFF}$ are increasing for $V_{\rm TG} < 0$ V [11], [28]. We speculate that the absence of the hole accumulation layer in a-IGZO is responsible for this difference.

The nonexistence of holes will make the formation of p-channel a-IGZO transistors impossible [29], [30] and will allow for the electric field generated by $V_{\rm TG}$ to penetrate into

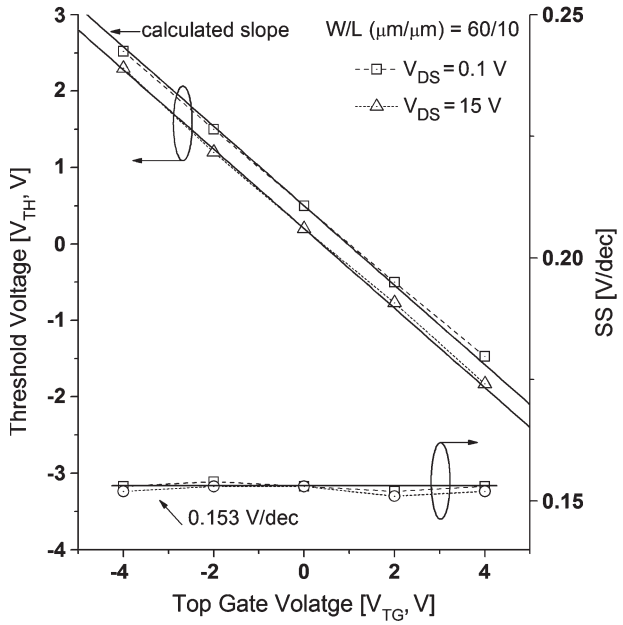

Fig. 8. $V_{\rm TH}$ and SS variation with the TG voltages $V_{\rm TG}$ of coplanar homojunction DG a-IGZO TFTs. The solid line represents the calculated curve using (20).

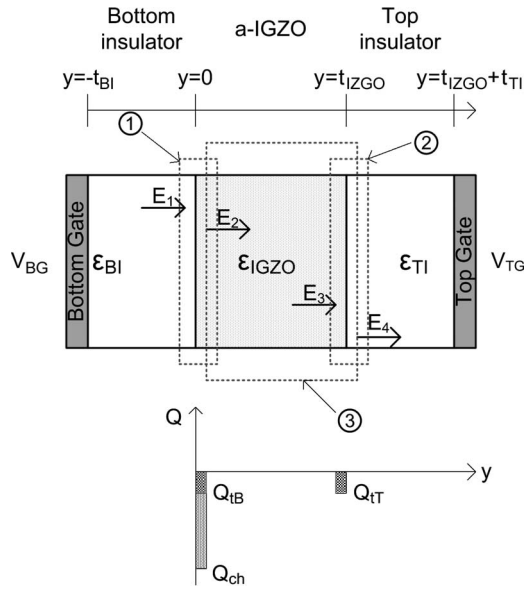

Fig. 9. Simplified cross-sectional view of DG TFT and space charge distribution.

the bottom channel. Consequently, a mutual interaction between the electric field generated by $V_{\rm TG}$ and $V_{\rm BG}$ is possible. Hence, $V_{\rm TG}$ will be responsible for band bending at the bottom interface, resulting in inhibition of the electron accumulation. Therefore, $V_{\rm TH}$ is expected to shift to a more positive direction in response to $V_{\rm TG} < 0$ V. If the hole accumulation would be possible in a-IGZO, then it will take place at the top interface and will block the electric filed generated by $V_{\rm TG}$. Consequently, the bottom channel will be hardly affected by $V_{\rm TG}$. [31] Moreover, the hole accumulation layer could change $I_{\rm OFF}$ and SS by generating unwanted leakage current. There is no such change on $I_{\rm OFF}$ and SS in DG a-IGZO TFTs.

To quantify the relation between the $V_{\rm TH}$ shift and $V_{\rm TG}$, an analysis using a simplified device structure is proposed. Fig. 8 summarizes the dependence between $V_{\rm TG}$ and $V_{\rm TH}$, extracted from Fig. 7. As shown in the figure, the relationship between $V_{\rm TG}$ and $V_{\rm TH}$ is linear. A similar observation was already made for DG a-IGZO TFTs [11], [12]. The relationship between $V_{\rm TH}$ and $V_{\rm TG}$ can be derived from the simplified device structure shown Fig. 9. Applying Gauss' law to surface 1(①) yields

$$\varepsilon_{\rm IGZO}E_2 - \varepsilon_{\rm BI}E_1 = Q_{\rm tB} + Q_{\rm ch} \tag{7}$$

and from surfaces 2 and 3 (② and ③), we can derive the following equations:

$$\varepsilon_{\rm TI}E_4 - \varepsilon_{\rm IGZO}E_3 = Q_{\rm tT} \tag{8}$$

$$\varepsilon_{\rm TI}E_4 - \varepsilon_{\rm IGZO}E_2 = Q_{\rm tT} \tag{9}$$

where $Q_{\rm tB}$ and $Q_{\rm tT}$ are trap densities, including surface bulk states at the bottom and top a-IGZO surfaces, respectively. $Q_{\rm ch}$ is the mobile charge density of the a-IGZO film. E_1, E_2, E_3, and E_4 are the electric fields at the drawn points in Fig. 9.

As a next step, the difference of electric potential is expressed as the integral of the electric field $E(y) = -dV(y)/dy$, i.e.,

$$\int_{y0}^{y} E(y)dy = V(y_0) - V(y). \tag{10}$$

Integration of (10) from $\rm y_0 = -t_{BI}$ to $y = 0$ gives

$$t_{\rm BI}E_1 = (V_{\rm BG} - \Delta\varphi_B) - V_{\rm ch} \tag{11}$$

where $V_{\rm ch}$ is the voltage at the channel surface $(y = 0)$.

Since $C_{\rm BI} = \varepsilon_{\rm BI}/t_{\rm BI}$, we can write

$$\frac{\varepsilon_{\rm BI}E_1}{C_{\rm BI}} = (V_{\rm BG} - \Delta\varphi_B) - V_{\rm ch}. \tag{12}$$

In addition, the integration of (10) from $y_0 = 0$ to $y = t_{\rm IGZO} + t_{\rm TI}$ gives

$$\frac{\varepsilon_{\rm TI}E_4}{C_{\rm TI}} + \frac{\varepsilon_{\rm IGZO}E_3}{C_{\rm IGZO}} = V_{\rm ch} - (V_{\rm TG} - \Delta\varphi_T). \tag{13}$$

Here, $\Delta\varphi_B$ and $\Delta\varphi_T$ represent the work function difference of the a-IGZO film at TG and BG electrodes. If we substitute (7)–(9), and (12) into (13), then $Q_{\rm ch}$ is expressed as

$$\begin{aligned} Q_{\rm ch} = &- C_{\rm BI}V_{\rm BG} - \left(\frac{C_{\rm TI}C_{\rm IGZO}}{C_{\rm TI}+C_{\rm IGZO}}\right)V_{\rm TG} \\ &- Q_{\rm tB} - \frac{C_{\rm IGZO}}{(C_{\rm TI}+C_{\rm IGZO})}Q_{\rm tT} \\ &+ C_{\rm BI}\left(1 - \frac{C_{\rm TI}C_{\rm IGZO}}{C_{\rm BI}(C_{\rm TI}+C_{\rm IGZO})}\right)V_{\rm ch} \\ &+ C_{\rm BI}\Delta Q_B + \frac{C_{\rm TI}C_{\rm IGZO}}{(C_{\rm TI}+C_{\rm IGZO})}\Delta Q_T. \end{aligned} \tag{14}$$

When the TFT is turned on, we can let $Q_{\rm ch}=0$ and $V_{\rm BG}=V_{\rm TH}$. Therefore

$$\begin{aligned}0=&-C_{\rm BI}V_{\rm TH}-\left(\frac{C_{\rm TI}C_{\rm IGZO}}{C_{\rm TI}+C_{\rm IGZO}}\right)V_{\rm TG}\\&-Q_{\rm tB}-\frac{C_{\rm BI}C_{\rm IGZO}}{C_{\rm BI}(C_{\rm TI}+C_{\rm IGZO})}Q_{\rm tT}\\&+C_{\rm BI}\left(1-\frac{C_{\rm TI}C_{\rm IGZO}}{C_{\rm BI}(C_{\rm TI}+C_{\rm IGZO})}\right)V_{\rm ch}\\&+C_{\rm BI}\Delta Q_B+\frac{C_{\rm TI}C_{\rm IGZO}}{(C_{\rm TI}+C_{\rm IGZO})}\Delta Q_T.\end{aligned}\tag{15}$$

Moving the $-C_{\rm BI}V_{\rm TH}$ term to the left side and dividing both sides by $C_{\rm BI}$ and defining β as

$$\beta=-\frac{C_{\rm TI}C_{\rm IGZO}}{C_{\rm BI}(C_{\rm TI}+C_{\rm IGZO})}\tag{16}$$

then we obtain

$$V_{\rm TH}=-\beta V_{\rm TG}-\frac{Q_{\rm tB}}{C_{\rm BI}}-\frac{\beta}{C_{\rm TI}}Q_{\rm tT}+(1-\beta)V_{\rm ch}+\Delta Q_B+\beta\Delta Q_T.\tag{17}$$

β is a function of the capacitances, which is related to the a-IGZO and the gate insulator thickness. From Table I, $C_{\rm TI}$ and $C_{\rm BI}$ are 9.5 and 17.7 nF/cm^2, respectively. In addition, $C_{\rm IGZO}$ is 295 nF/cm^2 for $\varepsilon_{\rm IGZO}=10\cdot\varepsilon_0$ and $t=30$ nm, then we can calculate $\beta=-0.52$ for the device used in this paper.

For more simplification, we define $V_{\rm TH}(0)$ as

$$V_{\rm TH}(0)=-\frac{Q_{\rm tB}}{C_{\rm BI}}-\frac{\beta}{C_{\rm TI}}Q_{\rm tT}+(1-\beta)V_{\rm ch}+\Delta Q_B+\beta\Delta Q_T.\tag{18}$$

$V_{\rm TH}(0)$ is considered as the TFT's threshold voltage for TG voltage $V_{\rm TG}=0$ V.

Finally, the relation between $V_{\rm TH}$ and $V_{\rm TG}$ can be expressed in a simple linear form

$$V_{\rm TH}=V_{\rm TH}(0)+\beta V_{\rm TG}.\tag{19}$$

The solid line in Fig. 8 represents (19) for $\beta=-0.52$. The derived equation is in good agreement with the experimental data. A similar observation has been made for DG a-IGZO TFT with $L=5$ μm. This good agreement between calculated and experimental data supports the proposed model shown in Fig. 9.

According to (16), β is dependent on the thickness of TG/BG insulators and the a-IGZO layer. If the a-IGZO channel layer is very thin, then (16) is simplified to $\beta=-C_{\rm TI}/C_{\rm BI}$ and $\beta=-0.53$ for the values of $C_{\rm TI}=9.5$ and $C_{\rm BI}=17.7$ nF/cm^2, which is very close to the experimental value of -0.52 obtained from Fig. 8. Since the a-IGZO film used in this paper is very thin, therefore the shift of $V_{\rm TH}$ is expected to mostly be influenced by $C_{\rm TI}$ and $C_{\rm BI}$.

We also investigated the DG TFT characteristics under illumination. Fig. 10(a) shows the a-IGZO transfer characteristic without TG under illumination. We have shown in [19] that the illumination with $\lambda>\lambda_{\rm TH}$ generates the electron–hole pairs that will affect the TFT electrical characteristics; $\lambda_{\rm TH}$ is the threshold wavelength that is closely related to the optical bandgap. No major changes occur in the wavelength range $\lambda>420$ nm (2.95 eV). A significant change in $I_{\rm OFF}$, SS, and $V_{\rm TH}$ takes place only for $\lambda<420$ nm. We confirmed that, under illumination of a-IGZO TFT without TG, hysteresis, $I_{\rm OFF}$, and SS are increasing; hysteresis (0 to 2 V), $I_{\rm OFF}$ (0.1 to 10 pA), and SS (153 to 388 mV/dec). These results are in agreement with [19]. From this result, it is clear that although a-IGZO is transparent in a given photon energy range, for its application to AM-FPD, the light shield is needed to prevent $I_{\rm OFF}$ increase. In the DG TFT structure, the TG metal electrode, as shown in Fig. 1, can serve as light shield and protect the channel area from illumination. Fig. 10(b) shows the DG TFT transfer characteristics in the dark and under broadband illumination. We note that the two curves are identical. Therefore, the introduction of the TG effectively protects the channel area from illumination and maximizes the light stability of a-IGZO DG TFTs. At the same time, the DG TFT provides superior electrical characteristics in comparison with the single-gate TFT.

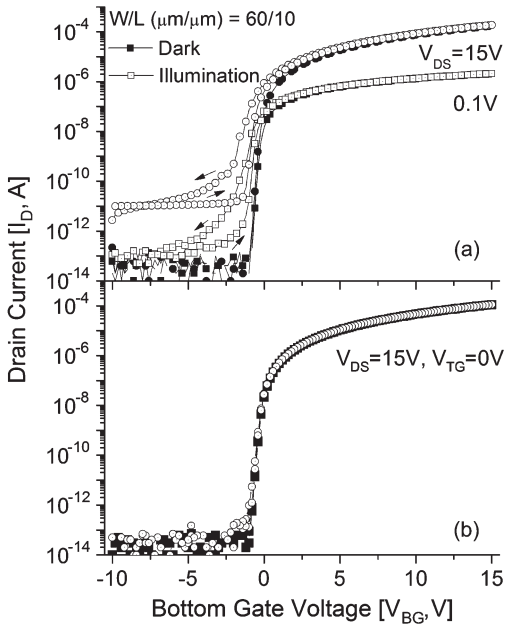

Fig. 10. Transfer characteristic of coplanar homojunction a-IGZO TFTs without and with TG structure in the dark and under illumination.

IV. Application of DG a-IGZO TFT to AM-OLEDs

The a-IGZO TFT is emerging today as a strong candidate for a pixel circuit in AM-OLEDs because of its remarkable merits, such as high mobility, low off current, high electrical stability, and low temperature fabrication requirements. Aside from these advantages, DG a-IGZO TFTs show even higher on-current capability, a sharper SS, excellent controllability of the threshold voltage, good electrical stability, and excellent light stability. These characteristics make DG a-IGZO TFTs a very attractive candidate for AM-OLED.

The simple pixel circuit in AM-OLED includes at least two TFTs with one storage capacitor $C_{\rm ST}$ [32]. In a traditional two-TFT pixel circuit [Fig. 11(a)], when the switching TFT $T_{\rm SW}$ is

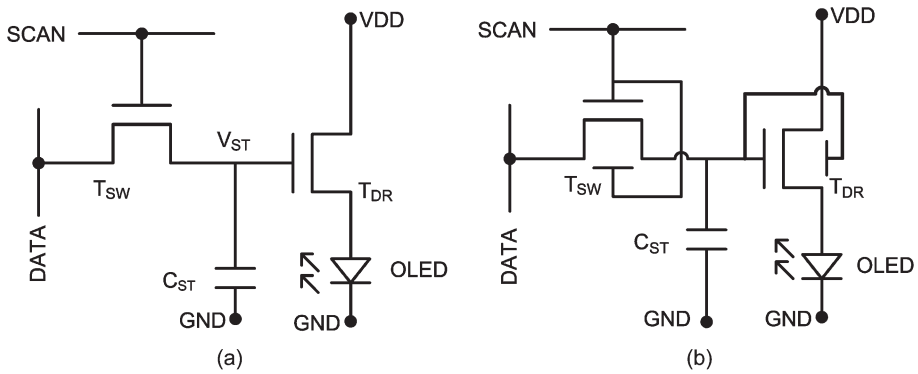

Fig. 11. (a) Traditional AM-OLED pixel driving circuit. (b) Proposed AM-OLED pixel driving circuit based on DG TFT to be used as switching and driving transistors.

turned on during the programming stage, the data signal voltage is stored at $C_{\rm ST}$ through $T_{\rm SW}$, generating the node voltage $V_{\rm ST}$ on $C_{\rm ST}$. Once the programming stage is completed, $T_{\rm SW}$ is turned off during the retention stage. $V_{\rm ST}$ at the gate of the driving TFT $T_{\rm DR}$ maintains a constant current, which flows through $T_{\rm DR}$.

For the AM-OLED pixel circuit, two TFT properties are important: 1) the programming speed and 2) the retention period. The programming speed of the pixel circuit is the time required to charge $C_{\rm ST}$ to the desired $V_{\rm ST}$. A lengthy required time may result in insufficient charging of $C_{\rm ST}$, thereby causing an error in the display gray scale [33]. To maximize the charging performance, it is necessary for $T_{\rm SW}$ to have a high $I_{\rm ON}$ and a fast switching capability between on and off states. Since DG a-IGZO TFT has a high ON-current and a small SS, it is expected that $T_{\rm SW}$ will have an enhanced pixel charging performance.

Second, the retention period is also critical for AM-OLEDs. The retention period is the time that $C_{\rm ST}$ retains the electrical charges, and these charges stored in $C_{\rm ST}$ can leak out through a leakage current of $T_{\rm SW}$ during this stage. The $C_{\rm ST}$ charge loss causes display gray scale distortion. To prevent such distortion, TFTs having a low leakage current are desired. It is clear from this paper that a-IGZO has a smaller leakage current than a-Si:H or poly-Si TFTs, which are currently the most widely used AM-OLED pixel circuits. Moreover, this paper has demonstrated that the leakage current of the DG a-IGZO TFT is constant under different bias conditions and even under BTS or light illumination (when the TG is present). Therefore, overall, we can expect an excellent electrical performance of the DG a-IGZO TFT pixel circuit. Fig. 11(b) shows an example of the AM-OLED pixel circuit based on DG a-IGZO TFTs. Unlike the case in normal TFT structure, the TFT's TG and BG are connected together in the proposed pixel circuit. For dynamic control of the TFT threshold voltage, the TG should be biased separately, which requires an additional control line.

V. Conclusion

The DG coplanar homojunction a-IGZO TFT has been fabricated, and its electrical characteristics and stability have been described. We confirmed that this device has a good ohmic S/D contact. Under DG bias conditions, the TG and BG electrodes form two conduction channel layers at the top and bottom interfaces. A high $I_{\rm ON}$ and a steep SS are achieved without increasing $I_{\rm OFF}$ and $\Delta V_{\rm TH}$. We showed that the lack of hole accumulation in the a-IGZO TFT is the basis for the linear dependence of the threshold voltage on TG voltages while the other device parameters are unchanged. This linear relationship is verified by Gauss's law using the proposed simplified DG TFT model. The threshold voltage shifts of about $+4.5$ and ± 0.2 V are observed during PBTS and NBTS, respectively, at 80 °C. Additionally, the TG is an excellent light shield, which ensures TFT stability under light illumination. The observed electrical properties and stability make the DG a-IGZO TFT a strong candidate for AM-OLED pixel circuits.

References

[1] J.-H. Lee, D.-H. Kim, D.-J. Yang, S.-Y. Hong, K.-S. Yoon, P.-S. Hong, C.-O. Jeong, H.-S. Park, S.Y. Kim, S.K. Lim, S.S. Kim, K.-S. Son, T.-S. Kim, J.-Y. Kwon, and S.-Y. Lee, "42.2: World's largest (15-inch) XGA AMLCD panel using IGZO oxide TFT," in *Proc. SID Symp. Dig. Tech. Papers*, 2008, vol. 39, pp. 625–628.

[2] J. K. Jeong, J. H. Jeong, J. H. Choi, J. S. Im, S. H. Kim, H. W. Yang, K. N. Kang, K. S. Kim, T. K. Ahn, H.-J. Chung, M. Kim, B. S. Gu, J.-S. Park, Y.-G. Mo, H. D. Kim, and H. K. Chung, "3.1: Distinguished Paper: 12.1-Inch WXGA AMOLED display driven by indium–gallium–zinc oxide TFTs array," in *Proc. SID Symp. Dig. Tech. Papers*, 2008, vol. 39, pp. 1–4.

[3] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, Nov. 2004.

[4] H. Kumomi, S. Yaginuma, H. Omura, A. Goyal, A. Sato, M. Watanabe, M. Shimada, N. Kaji, K. Takahashi, M. Ofuji, T. Watanabe, N. Itagaki, H. Shimizu, K. Abe, Y. Tateishi, H. Yabuta, T. Iwasaki, R. Hayashi, T. Aiba, and M. Sano, "Materials, devices, and circuits of transparent amorphous-oxide semiconductor," *J. Display Technol.*, vol. 5, no. 12, pp. 531–540, Dec. 2009.

[5] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping $*$," *J. Display Technol.*, vol. 5, no. 12, pp. 468–483, Dec. 2009.

[6] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance," *IEEE Electron Device Lett.*, vol. EDL-8, no. 9, pp. 410–412, Sep. 1987.

[7] R. A. Street, X. D. Wu, R. Weisfield, S. Ready, R. Apte, M. Ngyuen, W. B. Jackson, and P. Nylen, "Two-dimensional amorphous silicon image sensor arrays," *J. Non-Cryst. Solids*, vol. 198–200, pp. 1151–1154, May 1996.

[8] M. J. Lee, C. P. Judge, and S. W. Wright, "Thin film transistors for displays on plastic substrates," *Solid State Electron.*, vol. 44, no. 8, pp. 1431–1434, Aug. 2000.

[9] P. Servati, K. S. Karim, and A. Nathan, "Static characteristics of a-Si:H dual-gate TFTs," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 926–932, Apr. 2003.
[10] K. S. Karim, A. Nathan, J. A. Rowlands, and S. O. Kasap, "X-ray detector with on-pixel amplification for large area diagnostic medical imaging," *Proc. Inst. Elect. Eng.—Circuits, Devices Syst.*, vol. 150, no. 4, pp. 267–273, Aug. 2003.
[11] K. Takechi, M. Nakata, K. Azuma, H. Yamaguchi, and S. Kaneko, "Dual-gate characteristics of amorphous $InGaZnO_4$ thin-film transistors as compared to those of hydrogenated amorphous silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 2027–2033, Sep. 2009.
[12] H. Lim, H. Yin, J.-S. Park, I. Song, C. Kim, J. Park, S. Kim, S.-W. Kim, C. B. Lee, Y. C. Kim, Y. S. Park, and D. Kang, "Double gate GaInZnO thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 6, pp. 063 505-1–063 505-3, Aug. 2008.
[13] J.-H. Choi, H.-S. Seo, and J.-M. Myoung, "Dual-gate InGaZnO thin-film transistors with organic polymer as a dielectric layer," *Electrochem. Solid-State Lett.*, vol. 12, no. 4, pp. H145–H148, 2009.
[14] K. Takechi, M. Nakata, T. Eguchi, H. Yamaguchi, and S. Kaneko, "Study on current crowding in the output characteristics of amorphous $InGaZnO_4$ thin-film transistors using dual-gate structures with various active-layer thicknesses," *Jpn. J. Appl. Phys.*, vol. 48, no. 8, p. 081 606, Aug. 2009.
[15] K.-S. Son, J.-S. Jung, K.-H. Lee, T.-S. Kim, J.-S. Park, Y.-H. Choi, J.-Y. Kwon, and S.-Y. Lee, "5.3: Improvement of bias stability and transfer characteristics by using double gate GaInZnO TFTs," in *Proc. Eurodisplay*, Rome, Italy, 2009.
[16] A. Sato, K. Abe, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, "Amorphous In–Ga–Zn–O coplanar homojunction thin-film transistor," *Appl. Phys. Lett.*, vol. 94, no. 13, p. 133 502, Mar. 2009.
[17] A. Sato, M. Shimada, K. Abe, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, "Amorphous In–Ga–Zn–O thin-film transistor with coplanar homojunction structure," *Thin Solid Films*, vol. 518, no. 4, pp. 1309–1313, Dec. 2009.
[18] D. P. Gosain and T. Tanaka, "Instability of amorphous indium gallium zinc oxide thin film transistors under light illumination," *Jpn. J. Appl. Phys.*, vol. 48, no. 3, p. 03B 018, Mar. 2009.
[19] T.-C. Fung, C.-S. Chuang, K. Nomura, H.-P. D. Shieh, H. Hosono, and J. Kanicki, "Photofield-effect in amorphous In–Ga–Zn–O (a-IGZO) thin-film transistors," *J. Inf. Display*, vol. 9, no. 4, pp. 21–29, Dec. 2008.
[20] J. Kanicki, F. R. Libsch, J. Griffith, and R. Polastre, "Performance of thin hydrogenated amorphous silicon thin-film transistors," *J. Appl. Phys.*, vol. 69, no. 4, pp. 2339–2345, Feb. 1991.
[21] T.-C. Fung, C.-S. Chuang, C. Chen, K. Abe, R. Cottle, M. Townsend, H. Kumomi, and J. Kanicki, "Two-dimensional numerical simulation of radio frequency sputter amorphous In–Ga–Zn–O thin-film transistors," *J. Appl. Phys.*, vol. 106, no. 8, p. 084 511, Oct. 2009.
[22] P. Ranade, Y.-C. Yeo, Q. Lu, H. Takeuchi, T.-J. King, and C. Hu, "Molybdenum as a gate electrode for deep sub-micron CMOS technology," in *Proc. Mater. Res. Soc. Symp.*, 2000, vol. 611, p. C3.2.1.
[23] T.-C. Fung, K. Abe, H. Kumomi, and J. Kanicki, "Electrical instability of RF sputter amorphous In–Ga–Zn–O thin-film transistors," *J. Display Technol.*, vol. 5, no. 12, pp. 452–461, Dec. 2009.
[24] G. Baek, A. Kuo, J. Kanicki, K. Abe, and H. Kumomi, "P-11: Electrical properties and stability of dual-gate coplanar homojunction amorphous indium–gallium–zinc–oxide thin-film transistor," in *Proc. Soc. Inf. Display*, Los Angeles, CA, 2011, pp. 1136–1139.
[25] K. Abe, K. Takahashi, A. Sato, H. Kumomi, K. Nomura, T. Kamiya, J. Kanicki, and H. Hosono, "Analysis of current-voltage characteristics and electrical stress instabilities in amorphous In–Ga–Zn–O dual-gate TFTs," *IEEE Trans. Electron Devices*, submitted for publication.
[26] H. S. P. Wong, "Beyond the conventional transistor," *IBM J. Res. Develop.*, vol. 46, no. 2/3, pp. 133–168, Mar. 2002.
[27] F. R. Libsch and J. Kanicki, "A new threshold voltage shift estimation method for bias-temperature stress of amorphous silicon thin-film transistors," in *Proc. Jpn. Display*, 1992, pp. 443–446.
[28] Y. Kaneko, K. Tsutsui, and T. Tsukada, "Back-bias effect on the current-voltage characteristics of amorphous silicon thin-film transistors," *J. Non-Crystal. Solids*, vol. 149, no. 3, pp. 264–268, Nov. 1992.
[29] M. Orita, H. Tanji, M. Mizuno, H. Adachi, and I. Tanaka, "Mechanism of electrical conductivity of transparent $InGaZnO_4$," *Phys. Rev. B, Condens. Matter*, vol. 61, no. 3, pp. 1811–1816, Jan. 2000.
[30] K. Kobayashi, Y. Kohno, Y. Tomita, Y. Maeda, and S. Matsushima, "Possibility for hole doping into amorphous $InGaZnO_4$ films prepared by RF sputtering," *Phys. Stat. Sol. (C)*, vol. 8, no. 2, pp. 531–533, Feb. 2011.
[31] H.-K. Lim and J. G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFETs," *IEEE Trans. Electron Devices*, vol. ED-30, no. 10, pp. 1244–1251, Oct. 1983.
[32] T. P. Brody, F. C. Luo, Z. P. Szepesi, and D. H. Davies, "A 6 × 6-in 20-lpi electroluminescent display panel," *IEEE Trans. Electron Devices*, vol. ED-22, no. 9, pp. 739–748, Sep. 1975.
[33] H. Lee, C.-S. Chiang, and J. Kanicki, "Dynamic response of normal and corbino a-Si:H TFTs for AM-OLEDs," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2338–2347, Sep. 2008.

Gwanghyeon Baek received the B.S. degree in physics from Korea University, Seoul, Korea, in 2002 and the M.S. degree in electrical engineering from Seoul National University, Seoul, in 2004. He is currently working toward the Ph.D. degree with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor.

From 2004 to 2007, he was an Engineer with Samsung Electronics, Yongin, Korea. His research mainly focuses on a-InGaZnO TFTs and their application to active-matrix imagers or displays.

Katsumi Abe received the B.S. and M.S. degrees in nuclear engineering from Kyoto University, Kyoto, Japan, in 1993 and 1995, respectively.

He has been with the Canon Research Center, Canon Inc., Tokyo, Japan, since 2003. His research focuses on amorphous oxide semiconductor TFTs and their device physics.

Alex Kuo received the B.S. degree in electrical engineering from the University of California, Berkeley, in 2002 and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 2003 and 2008, respectively.

He is currently with the Displays and Detectors Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan. His research interests include a-Si:H TFTs for FPD and device physics for TFT.

Hideya Kumomi received the B.S., M.S., and Dr. Sci. degrees in physics from Waseda University, Tokyo, Japan.

He has been with Canon Research Center, Canon Inc., Tokyo, for about two decades. He has been working on nonlinear phenomena in phase transition, particularly on nucleation problems, and on TFTs based upon single-crystalline or polycrystalline Si and amorphous oxide semiconductors. He currently manages a laboratory for oxide semiconductors at Canon Inc. and also serves as Committee Member of technical conferences and an Editor of scientific journals.

Jerzy Kanicki received the Ph.D. degree in sciences (D.Sc.) from the Free University of Brussels (ULB), Brussels, Belgium, in 1982. His dissertation research work involved the "optical, electrical, and photovoltaic properties of undoped and doped trans-polyacetylene."

He subsequently joined the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, as a Research Staff Member working on hydrogenated amorphous silicon devices for photovoltaic and flat-panel display applications. In 1994, he moved from IBM Research Division to the Department of Electrical Engineering and Computer Science, University of Michigan, as a Professor. At the University of Michigan from 1994 to 2000, he did leading work on various flat-panel display technologies. He started research work in 2000 on a variety of fundamental problems related to organic and molecular electronics. Today, he is mainly interested in metal–oxide–semiconductor-based devices for displays and sensors. From 2002 to 2003, he spent a sabbatical year with the Center for Polymers and Organic Solids (Physics Department), University of California, Santa Barbara, conducting research in the area of conducting polymer devices. From 2009 to 2010, he spent a sabbatical year with the California Institute for Telecommunications and Information Technology, University of California, San Diego, doing research in the area of inorganic solar cells and chemical sensors based on organic thin-film transistors. He is the author and coauthor of over 250 publications in journals and conference proceedings. He has edited two books and three conference proceedings. He is coauthor of the book *High-Fidelity Medical Imaging Displays* (Bellingham, Washington: SPIE Press, 2004).

Dr. Kanicki presented numerous invited talks at national and international meetings in the area of organic and inorganic semiconductor devices. More information about his research group activities can be found at www.eecs.umich.edu/omelab/.